FPGA-based Implementation of Signal Processing for Through Wall Imaging Radar

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Abstract:
This paper deals with the implementation of signal processing sub-system of Through Wall Imaging Radar. Conventional SFCW Imaging radars use frequency domain backprojection for imaging which requires enormous computational resources. The paper proposes approximation of frequency domain backprojection algorithm using matched filtering, interpolation and time domain backprojection which has improved the imaging rate significantly. The design employs eight 16 bit ADCs and very high performance Xilinx FPGA device Kintex-7 XC7K 480T having several on-chip resources. Experimental results of the FPGA implementation are also presented.

Index Terms — SFCW, Matched filter, Back Projection, FPGA, Digital down conversion

I. INTRODUCTION

Through Wall Imaging Radar [1] is an ultra wideband radar technology used to detect and locate human beings behind walls during security and rescue operations. The radar can be operated over all standard non metallic walls. The two main sub systems of the radar are RF sub-system and digital signal processing sub-system. RF sub-system consists of waveform generator, transmitters with switch matrix, multichannel receivers and wideband antenna system. Digital signal processing sub-system consists of FPGA for data acquisition, down conversion and image construction. FPGA transfers image frames to CPU for further image processing. CPU realizes HMI and display image of static and moving targets.

FPGA design and implementation of signal processing algorithms [2] must be optimized to minimize computational overhead both in terms of processing and memory requirements so that real-time imaging is possible on modest hardware. Functionalities of FPGA include acquiring multiple ADC (16-bit) data synchronously, down conversion, calibration and windowing of acquired data, and execution of computationally intensive matched filtering, time domain back projection algorithm and coherence factor multiplication.

The paper is organized as follows. Data flow diagram of signal processor is presented in section II. Data acquisitions from multiple receive channels and digital down conversion of SFCW IF signal is given in section III. FPGA implementation of calibration using a reference channel and windowing to reduce side lobes are presented in Section IV. Section V describes FPGA design and implementation of backprojection algorithm which constructs the TWIR image. Image data transfer from FPGA to ARM core is explained in Section VI and the work is concluded in Section VII.

II. TWIR SIGNAL PROCESSOR

The main objectives of TWIR signal processor are to enhance the signal to noise ratio and to achieve high resolution in range and azimuth. This is achieved through two stages of processing, range compression followed by 2D Imaging. The data flow diagram of TWIR signal processor is shown in figure 1 and 2.

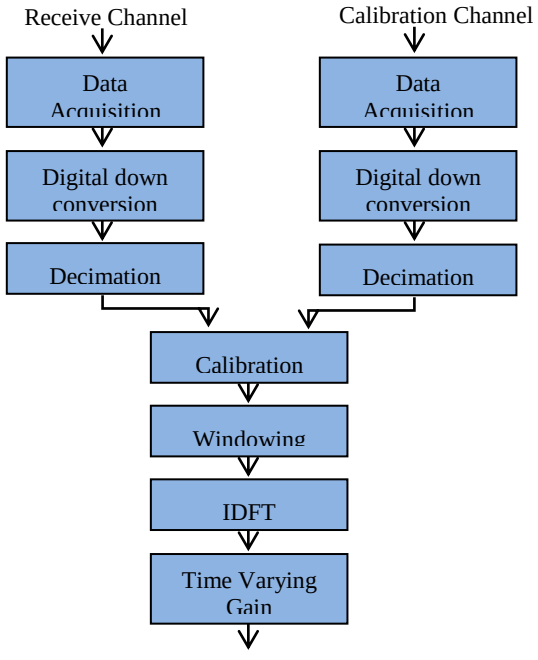

Figure 1 Range compression scheme

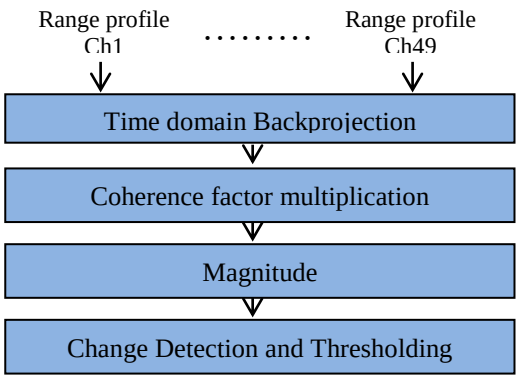

Figure 2 2D Imaging scheme

III. DIGITAL DOWN CONVERSION

ADCs are configured over SPI interface and Clock synthesizer CDCM6208 is programmed for 16 MHz ADC sampling clock. Digital data from each ADC channel is output over 16 I/O lines and is delivered into Xilinx Kintex 7 FPGA for signal processing. Digital down conversion (DDC) performs frequency translation needed to extract the amplitude and phase information for each spot frequency in SFCW waveform. It converts the digitized IF signal down to a baseband complex signal centered at zero frequency. 8 channels of Input data (7 receive channels and one loop back channel) at 16MHz is multiplexed and fed to the DDC. Internal operation of DDC is 8 times faster (at 128MHz speed) to cope with input data rate. DDC integrates a look up table which stores the complex reference IF sinusoid digitized at ADC sampling rate, a pair of mixers that translates IF to baseband and multi channel single stage FIR filter capable of converting 8 channels. Mixers are implemented using fixed point multipliers and multichannel FIR is realized using Xilinx IP LogiCORE FIR Compiler v5.0. Block diagram of multi channel DDC is shown in figure 3.

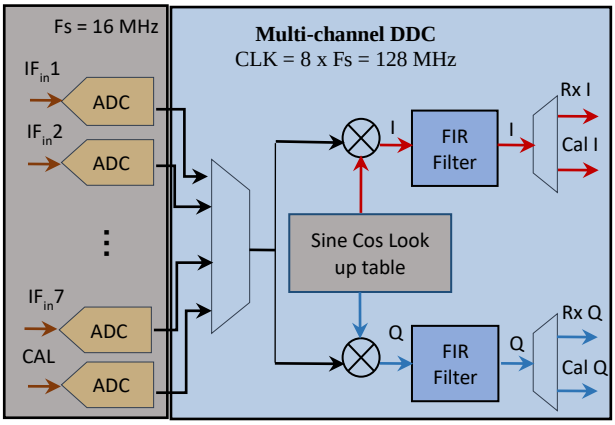

Figure 3 Multichannel Digital down conversion

IV. CALIBRATION AND WINDOWING

In heterodyne receiver, phase measurements are corrupted due to phase errors between the Tx and LO synthesizers. Phase errors are corrected using a reference channel that contains the same errors as the receive channel. Calibration procedure is mathematically illustrated in table 1.

	Receive channel	Reference channel
Transmit signal	$\sin(2\pi f_k t + \theta_k)$	$\sin(2\pi f_k t + \theta_k)$
LO signal	$\sin(2\pi(f_k + f_{IF})t + \theta_{LOk})$	$\sin(2\pi(f_k + f_{IF})t + \theta_{LOk})$
Received signal	$\sin(2\pi f_k(t - td) + \theta_k)$	$\sin(2\pi f_k(t - tc) + \theta_k)$
Baseband signal	$e^{-j(2\pi f_k td + \theta_{LOk} - \theta_k)}$	$e^{-j(2\pi f_k tc + \theta_{LOk} - \theta_k)}$
Corrected signal	$e^{-j2\pi f_k(td - tc)}$	

Table 1 Calibration procedure

Calibration is applied to all the seven Rx channels where each channel sample is divided by the respective sample from the reference channel. This is followed by applying Hamming Window to the calibrated data to reduce range side lobes. Weighted IQ data after calibration from 49 channels is stored in 14 BRAMs. Calibration and windowing are implemented using LogiCORE IP Floating-Point Operator v5.0. Figure 4 depicts the block diagram of calibration and windowing.

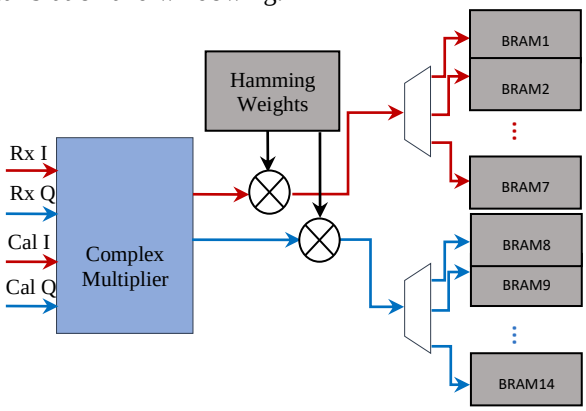

Figure 4 Calibration and windowing

V. IMAGING

SFCW based through wall imaging systems generally employ beamforming-on-receive scheme in frequency domain. Frequency domain backprojection algorithm (FD BP) performs 2D matched filtering and constructs target image from spatial and frequency samples of the received signals. The area to be imaged is divided into pixels and for each pixel backprojection [5] correlates the data collected at each transmit-receive position as a function of round trip time. Intensity at pixel p obtained by frequency domain backprojection is given by the equation

$$I(p) = \sum_{m=1}^{M}\sum_{n=1}^{N}\sum_{k=1}^{F} R_{mn,k} e^{j2\pi f_k \tau_{mn}(p)}$$

where $R_{mn,k}$ is the complex data received by mn^{th} Tx-Rx pair for k^{th} frequency, M is the number of transmit elements, N is the number of receive elements, F is the number of spot frequencies in SFCW waveform, $\tau_{mn}(p)$ is the round trip time from pixel p to mn^{th} Tx-Rx pair. The advantage of frequency domain backprojection over its time domain counterpart is the absence of rounding errors which gives a high quality image in terms of side lobes. But the disadvantage of frequency domain beamforming is the high computational complexity. For a 2D image consisting of 40000 pixels, 49 Tx-Rx pairs (channels) and 481 frequency points the number of complex multiplications and complex exponential evaluations required is 942760000 which require huge computing power for real time operation. In frequency domain backprojection equation the inner loop is doing range compression and the outer loops are performing the beamforming operation to extract cross range information for pixel p. Computational complexity can be reduced significantly by making the range compression independent on the number of pixels. Consequently two approaches have been analyzed

1) Range profile synthesis using IFFT and Time domain backprojection
2) Range profile synthesis using matched filter (correlation with transmit waveform) and Time domain backprojection

5.1 IFFT and Time domain backprojection (TD BP)

Time domain backprojection [2] performs the delay and sum beamforming on the spatial and temporal samples received by the 49 channels.

$$I(p) = \sum_{m=1}^{M}\sum_{n=1}^{N} S(mn, \tau_{mn}(p))$$

Range profile is synthesized using 512 point IFFT for the 49 channels and 2D image is constructed using time domain backprojection algorithm [4]. In TD BP, time delays are rounded to nearest time bin in the range compressed data. Large sampling interval in range compressed data produces significant rounding errors which lead to spreading of target in cross range. Rounding errors can be reduced by taking sufficient number of time samples. The image constructed using frequency domain backprojection is shown in figure 5. Figure 6 depicts the images obtained using IFFT of different lengths and TD BP.

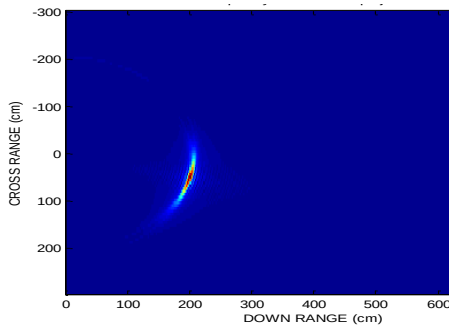

Figure 5 Image obtained using Frequency domain backprojection

There is significant difference between images obtained using frequency domain backprojection and that obtained using IFFT and TD BP. The reason is beamforming is frequency dependent and higher frequencies give a more focused image. The synthesis frequencies used by IFFT are 0, Δf, 2Δf…., (F-1)Δf but the SFCW transmitted frequencies are f_1, f_1+Δf, f_1+2Δf, ….., f_1+(F-1)Δf, where f_1 is the start frequency, F is the number of frequency spots and Δf is the step size of SFCW waveform. To correct the frequency mismatch the IFFT output is multiplied by a complex sinusoid of frequency f1 and figure 7 illustrates that the image obtained by the proposed method is similar to FD BP image.

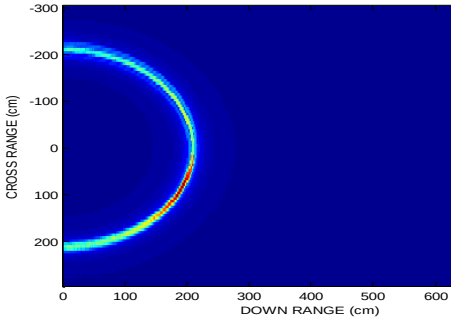

Figure 6(a) Image obtained using 512 point IFFT and time domain backprojection

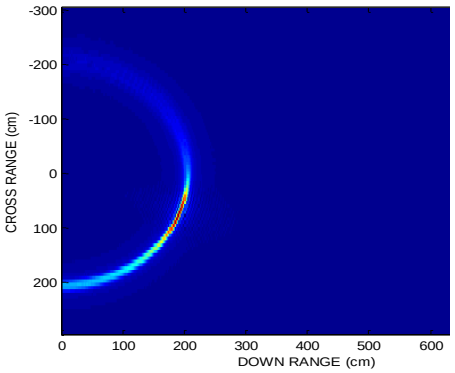

Figure 6(b) Image obtained using 8192 point IFFT and time domain backprojection

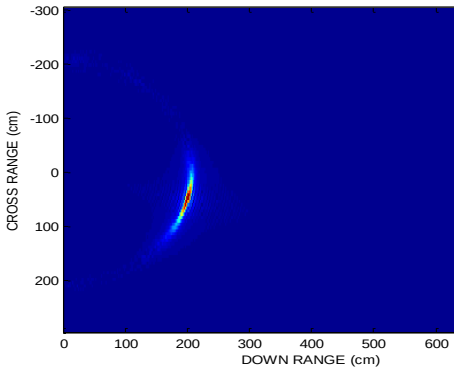

Figure 7 Image obtained using proposed method

5.2 Matched filtering and Time domain backprojection (TD BP)

In the second approach, the received SFCW IQ data is correlated with the complex conjugate of transmitted waveform to obtain the range compressed data.

$$S(mn, t_i) = \sum_{k=1}^{F} R_{mn,k}\, e^{j2\pi f_k t_i}$$

IFFT computes time samples between range 0 and maximum unambiguous range. If detection range is less than the unambiguous range matched filtering can be done only for time samples up to detection range with fewer number of time samples. The number of samples required depends on the area to be imaged and the accuracy of approximation of frequency domain backprojection. For an imaging area of 20 m x 10 m, 4000 time samples is selected based on simulation results.

5.3 Computational requirements

Approximation of frequency domain backprojection using the above two approaches reduces the computational requirements drastically. In the IFFT based approach complexity is reduced by a factor of 180 with 8192 point IFFT and in the second approach number of complex multiplications is reduced by one tenth of that in FD BP and number of complex exponential evaluations is reduced by a factor of 10 x N where N is the number of Tx-Rx pair data processed in parallel. In both methods the range compressed data for multiple channels has to be stored in memory. FPGA BRAM requirements in second approach is less compared to IFFT based approach and channel wise implementation of time domain

backprojection eliminate the need for storing range compressed data of all 49 channels simultaneously.

In order to reduce 49 channel range compression time, parallel implementation of multiple 'matched filter' cores are realized. Block diagram of partitioning range compression is shown in figure 8.

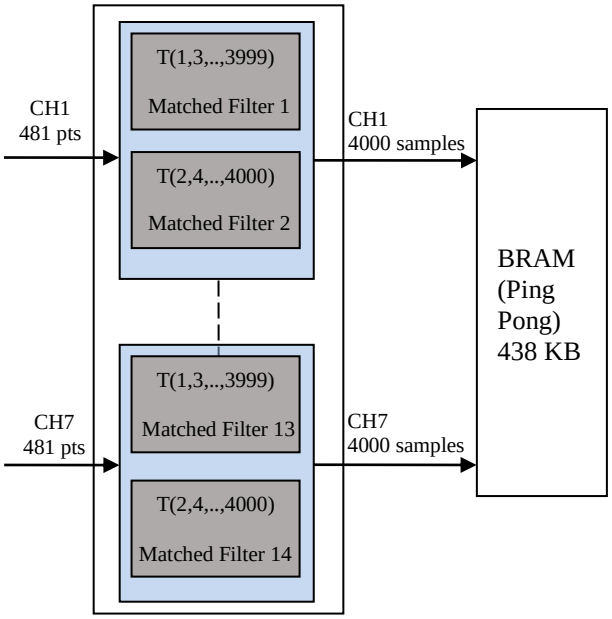

Figure 8 Multiple instantiation of matched filter

Backprojection module computes the delay of each pixel from each channel and sums the corresponding time samples which are stored in BRAM after range compression. The partial backprojected pixel values computed from 7 channel data are stored in BRAM and the process is repeated seven times (for 7 transmit channels) to get the final backprojected pixel values. Single core of backprojection is sufficient to meet the imaging requirement of 15frames/s. Matched filtering and Time domain backprojection are implemented using LogiCORE IP Floating-Point Operator v5.0, Fixed point IP core and BRAM.

5.4 Coherence factor multiplication

Coherence factor is used to suppress the low coherence features in the image such as target side lobes. It is the ratio of coherent power to the total power received by an array of receivers from a pixel and is given by

$$CF(p) = \frac{\left| \sum_{m=1}^{M} \sum_{n=1}^{N} S(mn, \tau_{mm}(p)) \right|^2}{\left| \sum_{m=1}^{M} \sum_{n=1}^{N} |S(mn, \tau_{mm}(p))| \right|^2}$$

Coherence factor is simply a measure of the relative coherence of the received signals across all channels and its value varies from 0 to 1. Backprojected value of a pixel is multiplied with its coherence factor to reduce the low coherence features like side lobes and noise as shown in figure 10. Coherence factor multiplication is realized in FPGA using an additional backprojection core and LogiCORE IP Floating-Point Operator v5.0.

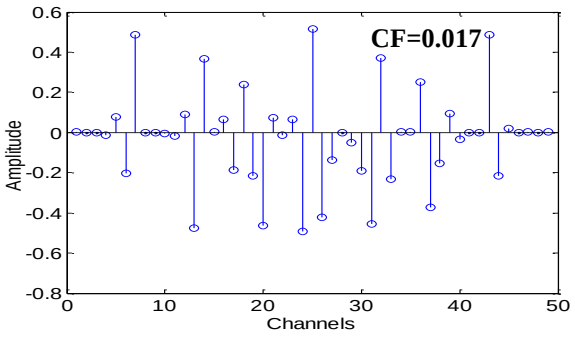

Figure 9(a) Samples (real part) received by 49 channels from non target pixel

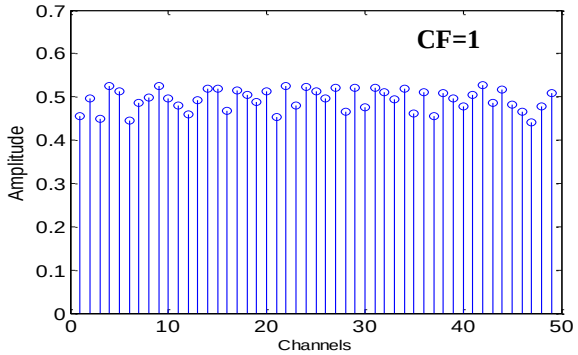

Figure 9 (b) Samples (real part) received by 49 channels from target pixel

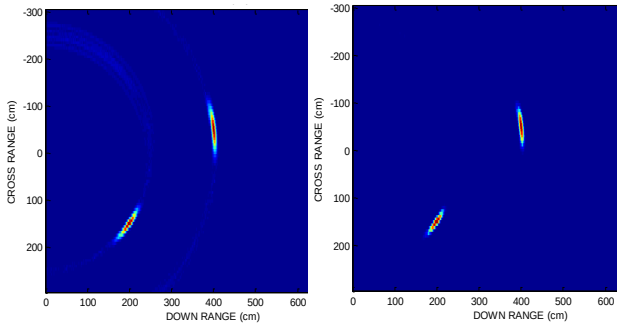

Figure 10 Effect of CF multiplication

5.5 Resource utilization

The device utilization summary of the implemented signal processing scheme on Kintex7 480T device is given in table 2.

Slice Logic Utilization	Used	Available	Utilization
Number of Slice Registers	81,973	597,200	14%
Number of Slice LUTs	56,178	298,600	19%
Number of occupied Slices	18,662	74,650	25%
Number of RAMB36E1/FIFO36E1s	472	955	50%
Number of DSP48E1s	576	1,920	30%

Table 2 Device utilization summary

VI. EMIF

Image data from FPGA is transferred to ARM for image processing over External memory interface (EMIF). EMIF connects ARM core to the FPGA, making the FPGA perform as a high-speed data processor. This design interface is a seamless connection to the FPGA FIFO. One

side of the FIFO communicates with the ARM core, while the other side communicates with internal FPGA logic. A FIFO to store 32 bit image data is built using the Xilinx CORE Generator™ tool.

VII. CONCLUSION

Through wall imaging radars require high processing power. The major contribution of this paper is to propose optimizations that reduce the enormous computing resources of the frequency domain backprojection algorithm and to improve the parallel efficiency of the system. The proposed signal processing implementation scheme was able to meet the real time imaging requirement of 15 frames per second on Kintex7 FPGA. IF signals from eight receiver channels are digitized using ADCs and multi channel digital down converter (DDC) is used taking into advantage of the low ADC sampling rate. Pipelining, parallelism and resource sharing are used to meet the resource and timing constraints of through wall imaging radar.

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